

RESEARCH ARTICLE

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Pwm Control Strategy For Controlling Of Parallel Rectifiers In Single Phase To Three Phase Drive System

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ABSTRACT:

This paper explains that how to develop and design, control of single phase to three phase drive system. The proposed topology of drive system consisting of two parallel connected rectifiers, inverter and induction motor, connected through inductor and capacitor, where used to produce balanced output to the motor drive. The main objective of this proposed method is to reduce the circulating currents and harmonic distortions at the converter input side, here the control strategy of drive system is PWM (pulse width modulations techniques) control strategy, the proposed topology also provides fault compensation in the case of short circuit faults and failure of switches for uninterrupted Power supplies. We also develop and simulate the MATLAB models for proposed drive system, by using MATLAB/ Simulink the output results simulate and observed.

I. INTRODUCTION

Power electronics drives widely used in all most all industries to drive different types of motors specially induction motors. Power electronics converters have been used to improve the power Capability, reliability, efficiency, and Redundancy. Electric utilities do not install three-phase power as a matter of course because it cost significantly more than single phase installation. Hence we need to conversion from single-phase to three-phase. Usually the operation of converters in parallel requires a transformer for isolation. However, weight, size, and cost associated with the transformer may make such a solution undesirable [1]. When an isolation transformer is not used, the reduction of circulating currents among different converter stages is an important objective in the system design

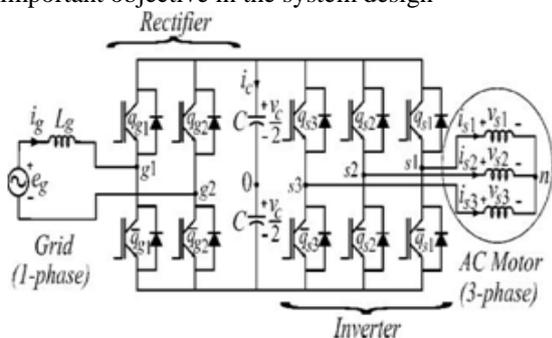


Fig. 1. Conventional single-phase to three-phase drive system

A single-phase to three-phase drive system composed of two parallel single-phase rectifiers and a three-phase inverter is proposed. The proposed system is conceived to operate where the single-phase utility grid is the unique option available. Compared to the conventional topology, the proposed system permits: to reduce the rectifier switch currents, the total harmonic distortion (THD) of the grid current

with same switching frequency or the switching frequency with same THD of the grid current; and to increase the fault tolerance characteristics. In addition, the losses of the proposed system may be lower than that of the conventional counterpart. The aforementioned benefits justify the initial investment of the proposed system, due to the increase of number of switches.

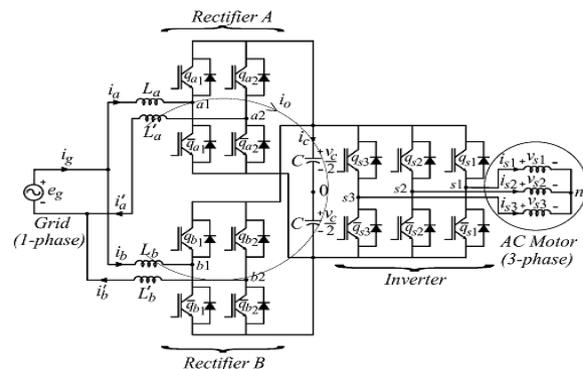


Fig 2 Modified (proposed) single-phase to 3-phase drive topology

II. SYSTEM MODEL

The system is composed of grid, input inductors ($L_a, L'_a, L_b,$ and $L'_b.$), rectifiers (A and B), capacitor bank at the dc link, inverter, and induction machine. Rectifiers A and B are constituted of switches $q_{a1}, \bar{q}_{a1}, q_{a2}$ and \bar{q}_{a2} and $q_{b1}, \bar{q}_{b1}, q_{b2}$ and \bar{q}_{b2} respectively the inverter is constituted of switches $\bar{q}_{s1}, q_{s2}, \bar{q}_{s2}, q_{s3}$ and \bar{q}_{s3} . The conduction state of the switches is represented by variables s_{qa1}, s_{qs3} , where $s_q = 1$ indicates a closed switch while $s_q = 0$ an open one. From Fig. 2, the following equations can be derived for the front-end rectifier

$$v_{a10} - v_{a20} = e_g - (r_a + l_a p)i_a - (r'_a + l'_a p)i'_a \quad (1)$$

$$v_{b10} - v_{b20} = e_g - (r_b + l_b p)i_b - (r'_b + l'_b p)i'_b \quad (2)$$

$$v_{a10} - v_{b10} = (r_b + l_b p)i_b - (r_a + l_a p)i_a \quad (3)$$

$$v_{a20} - v_{b20} = (r'_a + l'_a p)i'_a - (r'_b + l'_b p)i'_b \quad (4)$$

$$i_g = i_a + i_b = i'_a + i'_b \quad (5)$$

Where $p = d/dt$ and symbols like r and l represent the resistances and inductances of the input inductors L_a , L_b , and L'_b . The circulating current i_o can be defined from i_a and i'_a or i_b and i'_b and i.e.

$$i_o = i_a - i'_a = -i_b + i'_b \quad (6)$$

Introducing i_o and adding (3) and (4), Relations (1)—(4) become

$$v_a = e_g - [r_a + r'_a + (l_a + l'_a)p]i_a + (r'_a + p)i_o \quad (7)$$

$$v_b = e_g - [r_b + r'_b + (l_b + l'_b)p]i_b - (r'_b + l'_b p)i_o \quad (8)$$

$$v_o = -[r'_a + r'_b + (l'_a + l'_b)p]i_o - [r_a - r'_a + (l_a - l'_a)p]i_a + [r_b - r'_b + (l_b - l'_b)p]i_b \quad (9)$$

Where

$$v_a = v_{a10} - v_{a20} \quad (10)$$

$$v_b = v_{b10} - v_{b20} \quad (11)$$

$$v_o = v_{a10} + v_{a20} - v_{b10} - v_{b20} \quad (12)$$

Relations (7)—(9) and (5) constitute the front-end rectifier dynamic model. Therefore, v_a (rectifier A), v_b (rectifier B), and v_o (rectifiers A and B) are used to regulate currents i_a , i_b , and i_o , respectively. Reference currents i_a^* and i_b^* are chosen equal to $i_g^*/2$ and the reference circulating current i_o^* is chosen equal to 0. In order to both facilitate the control and share equally current, voltage, and power between the rectifiers, the four inductors should be equal, i.e., $r'_g = r_a = r'_a = r_b = r'_b$ and $l'_g = l_a = l'_a = l_b = l'_b$. In this case, the model (7)—(9) can be simplified to the model given by

$$v_a + \frac{v_o}{2} = e_g - 2(r'_g + l'_g p)i_a \quad (13)$$

$$v_b - \frac{v_o}{2} = e_g - 2(r'_g + l'_g p)i_b \quad (14)$$

$$v_o = -2(r'_g + l'_g p)i_o \quad (15)$$

Additionally, the equations for i_g , i'_a , i'_b can be written as

$$v_{ab} = \frac{v_a + v_b}{2} = e_g - (r'_g + l'_g p)i_g \quad (16)$$

$$v_a - \frac{v_o}{2} = e_g - 2(r'_g + l'_g p)i'_a \quad (17)$$

$$v_b + \frac{v_o}{2} = e_g - 2(r'_g + l'_g p)i'_b \quad (18)$$

In this ideal case (four identical inductors), the circulating current can be reduced to zero imposing

$$v_o = v_{a10} + v_{a20} - v_{b10} - v_{b20} = 0 \quad (19)$$

When $i_o = 0$ ($i_a = i'_a$, $i_b = i'_b$) the system model (7)-(9) is reduced to

$$v_a = e_g - 2(r'_g + l'_g p)i_a \quad (20)$$

$$v_b = e_g - 2(r'_g + l'_g p)i_b \quad (21)$$

Then, the model of the proposed system becomes similar to that of a system composed of two conventional independent rectifiers.

III. PWM STRATEGY

Considering that v_a^* , v_b^* , and v_o^* denote the reference voltages determined by the current controllers. i.e.

$$v_a^* = v_{a10}^* - v_{a20}^*, \quad (22)$$

$$v_b^* = v_{b10}^* - v_{b20}^*, \quad (23)$$

$$v_o^* = v_{a10}^* + v_{a20}^* - v_{b10}^* - v_{b20}^*, \quad (24)$$

The gating signals are directly calculated from the reference pole voltages v_{a10}^* , v_{a20}^* , v_{b10}^* , v_{b20}^* . Introducing an auxiliary variable $v_x^* = v_{a20}^*$ and solving this system of equations,

$$v_{a10}^* = v_a^* + v_x^* \quad (25)$$

$$v_{a20}^* = v_x^* \quad (26)$$

$$v_{b10}^* = \frac{v_a^*}{2} + \frac{v_b^*}{2} - \frac{v_o^*}{2} + v_x^* \quad (27)$$

$$v_{b20}^* = \frac{v_a^*}{2} - \frac{v_b^*}{2} - \frac{v_o^*}{2} + v_x^* \quad (28)$$

From these equations, it can be seen that, besides v_a^* , v_b^* and v_o^* , the pole voltages depend on also of v_x^* . The limit values of the variable v_x^* can be calculated by taking into account the maximum $v_c^*/2$ and minimum $-v_c^*/2$ value of the pole voltages

$$v_{x^*max} = (v_c^*/2) - v_{max}^* \quad (29)$$

$$v_{x^*min} = (-v_c^*/2) - v_{min}^* \quad (30)$$

Introducing a parameter μ ($0 \leq \mu \leq 1$), the variable v_x^* can be written as,

$$v_x^* = \mu v_{x^*max}^* + (1 - \mu) v_{x^*min}^* \quad (31)$$

Once v_x^* is chosen, pole voltages $v_{a10}^*, v_{a20}^*, v_{b10}^*$ and v_{b20}^* are defined from (4) to (7). The parameter μ changes the place of the voltage pulses related to v_a and v_b . And also μ influences the harmonic distortion of the voltages generated by the rectifier.

IV. SYSTEM CONTROL

The gating signals are obtained by comparing pole voltages with one ($vt1$), two ($vt1$ and $vt2$) or more high-frequency triangular carrier signals [17]–[20]. In the case of double-carrier approach, the phase shift of the two triangular carrier signals ($vt1$ and $vt2$) is 1800. The parameter μ changes the place of the voltage pulses related to v_a and v_b . When $v_x^* = v_{xmin}^* (\mu = 0)$ or $v_x^* = v_{xmax}^* (\mu = 1)$ are selected, the pulses are placed in the starting or in the ending of half period (T_s) of the triangular carrier signal.

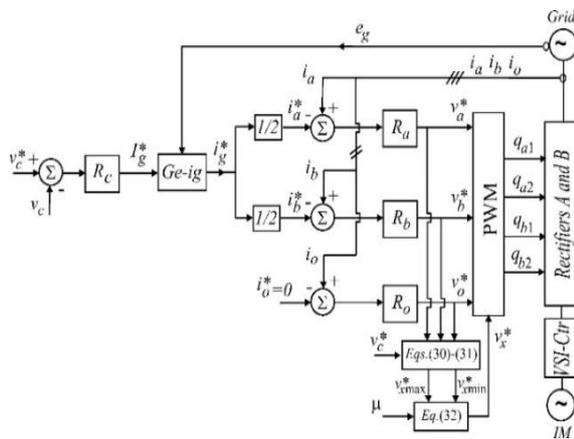


Fig. 3. Control block diagram.

The control block diagram of Fig3, highlighting the control of the rectifier. To control the dc-link voltage and to guarantee the grid power factor close to one. Additionally, the circulating current i_o in the rectifier of the proposed system needs to be controlled. In this way, the dc-link voltage v_c is adjusted to its reference value v_c^* using the controller R_c , which is a standard PI type controller. This controller provides the amplitude of the reference grid current I_g^* . To control power factor and harmonics in the grid side, the instantaneous reference current I_g^* must be synchronized with voltage e_g , as given in the voltage-oriented control (VOC) for three-phase system. This is obtained via blocks $G_e - i_g$, based on a PLL scheme. The reference currents i_a^* and i_b^* are obtained by making $i_a^* = i_b^* = I_g^*/2$, which means that each rectifier receives half of the grid current. The control of the rectifier currents is implemented using the Controllers indicated by blocks R_a and R_b . These Current controllers define the input reference voltages v_a^* and v_b^* . The homopolar current is measured

(i_o) and compared to its reference ($i_o^* = 0$). The error is the input of PI controller R_o that determines the Voltage v_o^* . The motor three-phase voltages are supplied from the inverter (VSI). Block VSI-Ctr indicates the inverter and its control. The control system is composed of the PWM command and a torque/flux control strategy (e.g., field-oriented control or volts/hertz control).

V. COMPARISION OF THD'S

Topology (PWM)	THDp/THDc
Proposed (S-Ca $\mu = 0.5$)	0.035
Proposed (D-Ca $\mu = 0.5$)	0.041
Proposed (D-Ca $\mu = 0$)	0.012

The dc-link capacitor current behavior is examined in this section. The proposed converter using double-carrier with $\mu = 0$ provides the best reduction of the high frequency harmonics. The highest reduction of THD is obtained for the converter using double-carrier with $\mu = 0$ and the THD obtained for $\mu = 1$ is equal to that for $\mu = 0$. By observing the above table we can say that the proposed method has lesser THD, when compared to conventional one. And also from the above table it is said that the THD of proposed one is lesser at double carrier $\mu=0$, when compared to single carrier $\mu=0.5$ and double carrier $\mu=0.5$.

VI. COMPENSATION OF FAULT

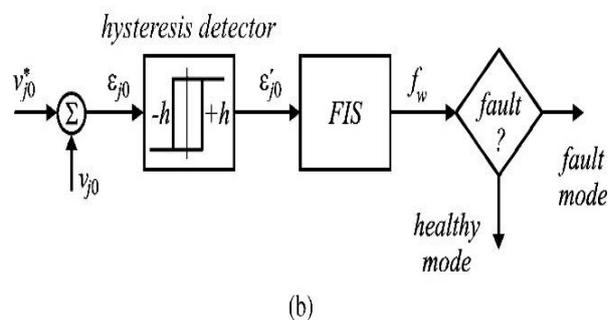


Fig.4. Proposed configuration highlighting devices of fault tolerant system

The fault compensation is achieved by reconfiguring the power converter topology with the help of isolating devices (fast active fuses— $F_j, j = 1, \dots, 7$) and connecting devices (back-to-back connected SCRs— $t1, t2, t3$), as observed in Fig. 4 and Discussed in [21]–[24]. These devices are used to redefine the post-fault converter topology, which allows continuous operation of the drive after isolation of the faulty power switches in the converter. Fig. 5 presents the block diagram of the

fault diagnosis system. In this figure, the block fault Identification system (FIS) detects and locates the faulty switches, defining the leg to be isolated. This control system is based on the analysis of the pole voltage error.

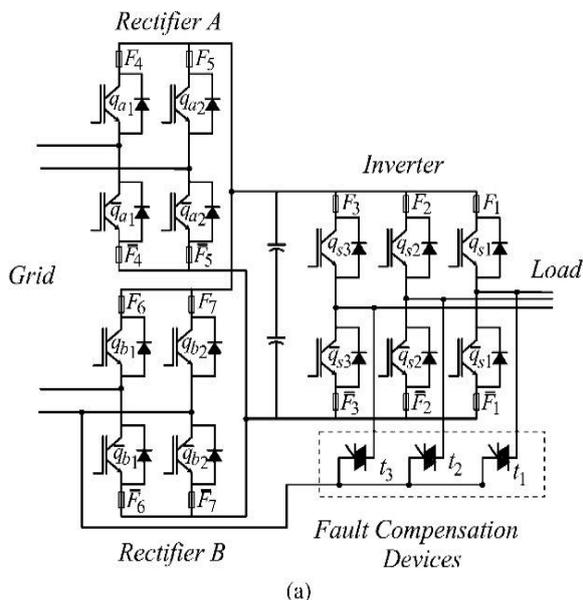


Fig.5. Block diagram of the fault diagnosis system

The proposed system can provide compensation for open-circuit and short-circuit failures occurring in the rectifier or inverter converter devices

The fault detection and identification is carried out in four steps:

- 1) Measurement of pole voltages ($v_j 0$);
- 2) Computation of the voltage error $\varepsilon_j 0$ by comparison of reference voltages and measurements affected in Step 1,
- 3) Determination as to whether these errors correspond or not to a faulty condition; this can be implemented by the hysteresis detector shown in Fig. 5,
- 4) Identification of the faulty switches by using $\varepsilon_{3j} 0$

This way, four possibilities of configurations have been considered in terms of faults:

- 1) Pre-fault (“healthy”) operation [see Fig. 6(a)];
- 2) Post-fault operation with fault at the rectifier B [see Fig. 6(b)];
- 3) Post-fault operation with fault at the rectifier A [see Fig. 6(c)];
- 4) Post-fault operation with fault at the inverter [see Fig. 6(d)].
- 5) When the fault occurrence is detected and identified by the control system, the proposed system is reconfigured and becomes similar to that in Fig. 1.

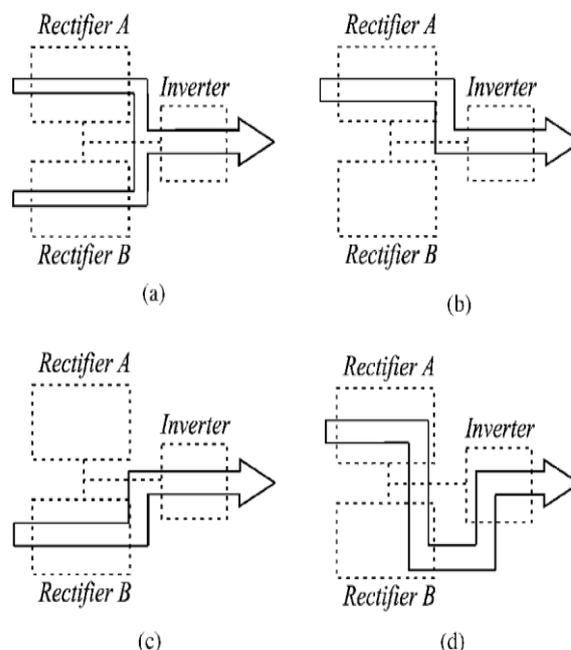


Fig. 6. Possibilities of configurations in terms of fault occurrence. (a) Pre-fault system. (b) Post-fault system with fault at the rectifier B. (c) Post-fault system with fault at the rectifier A. (d) Post-fault system with fault at the inverter.

VII. EFFICIENCY TABLE

	$\frac{\eta_p - 1}{\eta_c}$		
Frequency/Inductor	S-Ca $\mu = 0.5$	D-Ca $\mu = 0.5$	D-Ca $\mu = 0$
5 kHz/ ($L'g = Lg$)	-0.75%	-0.29%	1.61%

By observing the above table we can conclude that the efficiency of proposed system has better at D-Ca $\mu = 0$ as compared with the conventional system at the same operating conditions. The initial investment of the proposed system is higher than that of the standard one, since the number of switches and devices such as fuses and triacs is highest. But, considering the scenario when faults may occur, the drive operation needs to be stopped for a nonprogrammer maintenance schedule. The cost of this schedule can be high and this justifies the high initial investment inherent of fault-tolerant motor drive systems. On the other hand, the initial investment can be justified if the THD of the conventional system is a critical factor.

VIII. SIMULATION RESULTS

The proposed drive system is implemented by using MAT LAB SIMULINK TOOLS by connecting of blocks from mat lab library

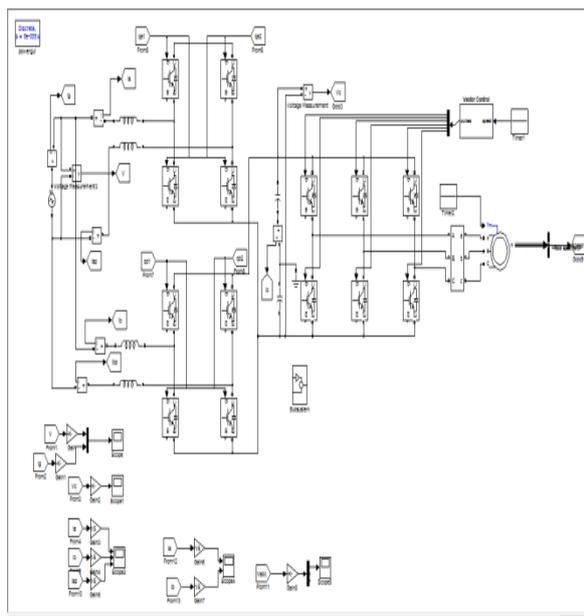
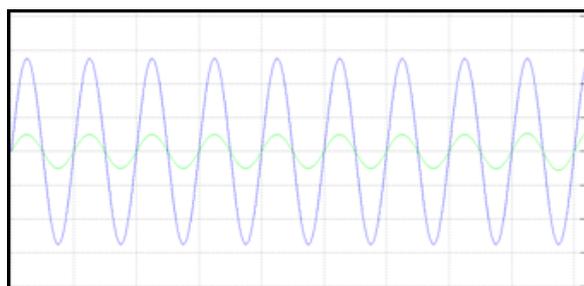
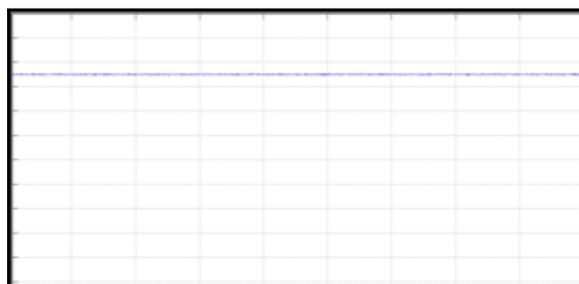


Fig.7: Mat lab model of proposed drive system

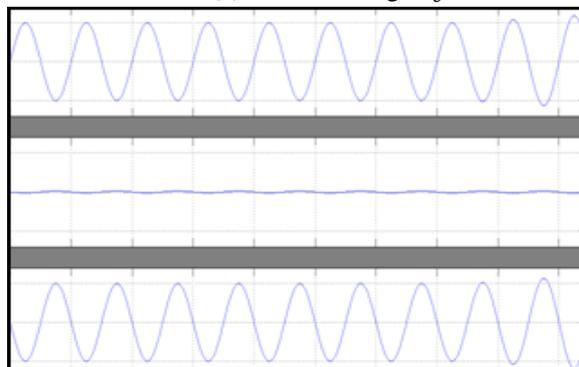
The steady-state experimental results are shown. The waveforms in this figure are: 8(a) voltage and current of the grid, 8(b) dc-link voltage, 8(c) currents of rectifier A and circulating current, 8.(d) currents of rectifiers A and B, and 8.(e) load line voltage. Note that, with the proposed configuration, all control demanded for single-phase to three-phase converter has been established. The control guarantees sinusoidal grid current with power factor close to one [see Fig.8.(a)], dc-link and machine voltages under control [see Fig.8.(b) and 8. (e)]. Furthermore, the proposed configuration provides current reduction in the rectifier side (half of the current of the standard topology) [see Fig. 8.(d)], which can provide loss reduction. Also, the control guarantees the circulating current close to zero [see Fig. 8. (c)]. The same set of experimental results was obtained for transient in the machine voltages, as observed in Fig. 9.(a) A volts/hertz control was applied for the three-phase machine, from $V/Hz = 83.3 \text{ V}/40 \text{ Hz}$ to $V/Hz = 125 \text{ V}/60 \text{ Hz}$ [see Fig. 9.(e)], which implies in increased of power furnished by



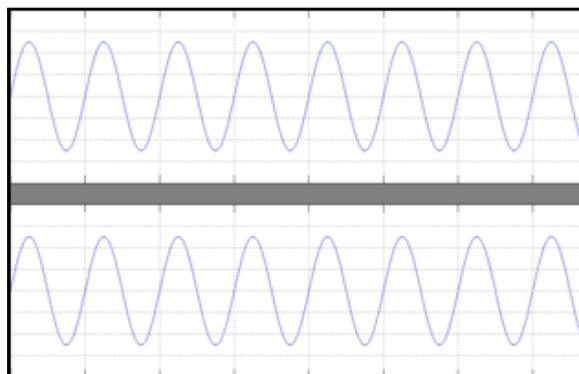
8. (a). Grid voltage v_g , grid current i_g



8. (b) dc-link voltage v_c



8. (c) Currents of rectifier A (i_a, i'_a) and circulating current (i_0).

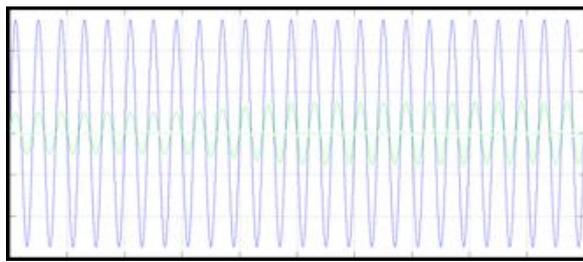


8. (d) Currents of rectifiers A (i_a) and B (i_b)

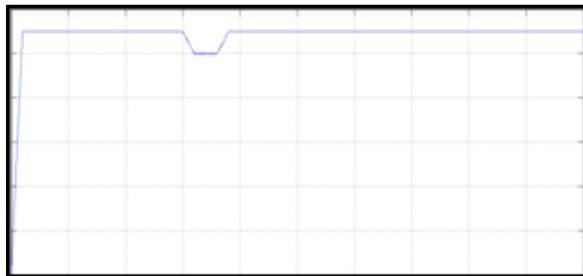


8. (e) load line voltage

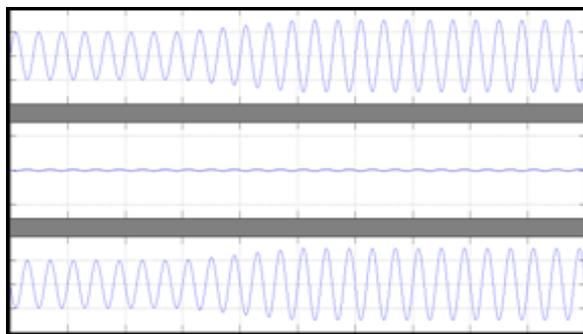
The below waveforms are Experimental results for a volts/hertz transient applied to the three phase motor. 9.(a) Grid voltage e_g and grid current i_g , 9.(b) Capacitor voltage (v_c), 9.(c) Currents of rectifier A and circulating current (i_0), 9.(d) Currents of rectifiers A (i_a) and B (i_b), 9.(e) Line voltage of the load.



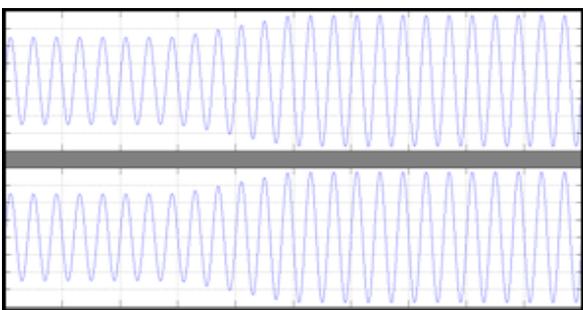
9.(a). Grid voltage v_g , grid current i_g



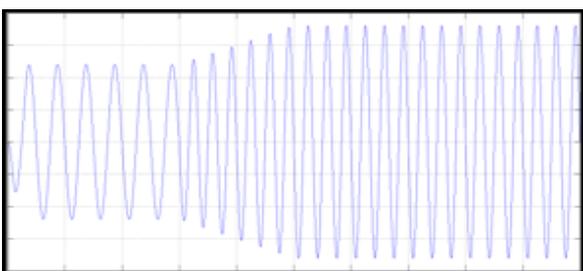
9. (b) dc-link voltage v_c



9. (c) Currents of rectifier A (i_a, i'_a) and circulating current (i_0).



9.(d) Currents of rectifiers A (i_a) and B (i_b)



9. (e) load line voltage

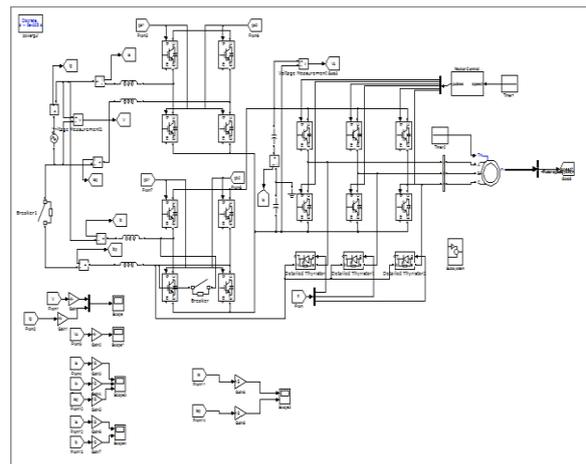
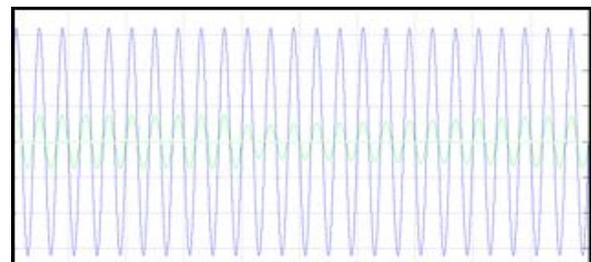
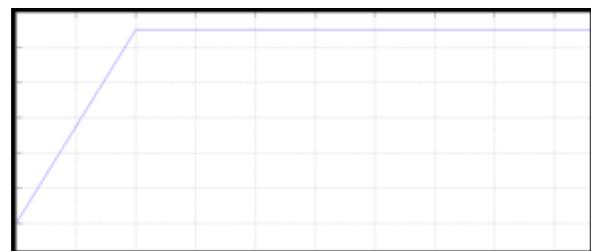


Fig 10: mat lab model of proposed system with fast acting switches for uninterrupted supplies when one of the rectifier switch filed

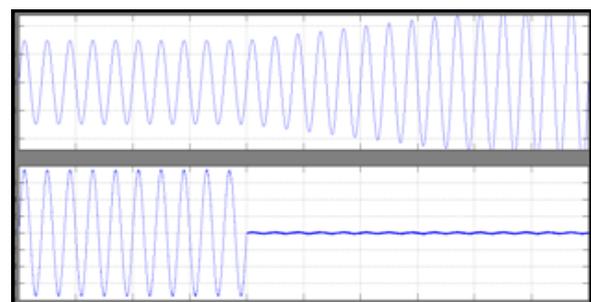
The below waveforms are in the case of failure of switch in B rectifier bridge 11(a).grid voltage v_g , and grid current i_g ,11(b). dc link voltage, v_c 11. (c) Currents of rectifiers A (i_a) and B (i_b), 11. (d) Currents of rectifier A (i_a, i'_a)



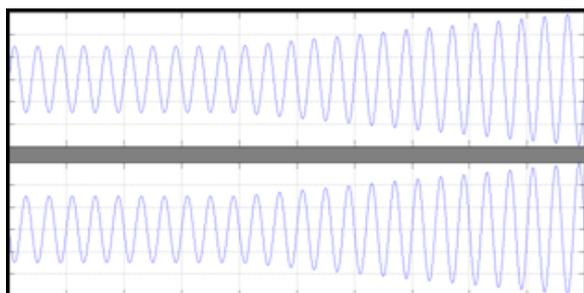
11. (a). Grid voltage v_g , grid current i_g



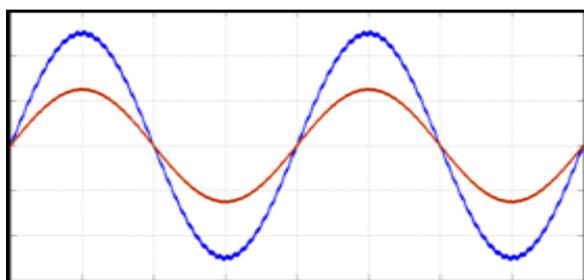
11. (b).dc link voltage v_c



11. (c) Currents of rectifiers A (i_a) and B (i_b)



11. (d) Currents of rectifier A (i_a, i'_a)



Simulation result highlighting the interleaved operation

IX. Conclusion

A single phase to three phase drive system combines two parallel rectifiers without the use of transformers. The system model and the control strategy, including the PWM technique, have been developed. The complete comparison between the proposed and standard configurations has been carried out. Compared to the conventional topology, the proposed system permits to reduce the rectifier switch currents, the *THD* of the grid current and to increase the fault tolerance characteristics. The simulation results have shown that the system is controlled properly, even with transient and occurrence of faults.

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